contact us: https://omdazz.aliexpress.com



Download the test code to FPGA

1 Open a project file

Open an existing FPGA project is simple: Copy the sample program which we provided to your hard disk, unzip files, please copy in the English directory, and no spaces.

Open Quartus II 11.0, select menu File -> Open Project



Open Proje	ct			8	×
查找范围(<u>t</u>):	01_led1) 💣 🏢 🔻	
ました (1) (1) (1) (1) (1) (1) (1) (1) (1) (1)	led1.qpf	tal_dh			
我的文档					
我的电脑					
	文件名 (M): 文件类型 (T):	Quartus II Project :	File (*.qpf *.qa		F (0) D消

After opening the project file, as shown below:

	menus Processing Io	is <u>window</u> Help	- √ - ₩ %	1 0 GB 20	1 🐼 🛲		Pets ET		80 L
Project Navigator	a@		led1.v					· ·	
Hierarchy	 ● ●	「 FPGA开发网 www.OurFPGA.co OurFPGA.taoba OurFPGA.degmail 家登陆网站,参当 、 、 、 文 件 期: 2011.0 : versio 法: led灯駆	om o.com o.com 与FPGA及电子材 信息****** 5.01 n 1.0 动实验	3 <table-cell> 253 支木讨论, 7</table-cell>	ab/	<u>→</u> 国 ⁴ 1	 .及资料 *******	*****	****
Tasks S X Flow: Compilati Customize Task Analysis 8 Analysis 8 Edit S View F Analysis 4 Norther Analysis 4 Norther	12 13 module 14 outp 15 as 16 // 17 18 endmodu 21	led1(led); ut[7:0] led; sign led=8'b0 assign led=8' le	0000000; /// b01010101;// //使用	京亮全部8个 对多个led 连续赋值语	·led 操作 句assig	n实现			

2 Download SOF file via JTAG interface

SOF file is downloaded using the JTAG port, the program will be lost after power-down:

infied	n - neon
cessing	Tools Window Help 🐬
led1	- 🐹 🖤 🖉 🧶 🐲 🕨 🕨 💌 😓 🧶 🖉 ም
	led1.v
$\mathbb{Q}_{\mathbb{B}} \overrightarrow{0}$	揮 揮 🔺 🌤 🌤 🎋 🖉 🖾 🔛 🇱 💩 🔜 🗉 😫
∃/**** **我们 **网站 **邮箱	************************************

Click "Hardware Setup" , then select "USB blaster".

Programmer	- F:/wx11/01	_led1/led1 - led	i1 - [l		X
<u>F</u> ile <u>E</u> dit <u>V</u> iew P <u>r</u> e	ocessing <u>T</u> ools <u>W</u> in	dow Help 🗣			
Hardware Setup	No Hardware	Mode: JTAG	6	▼ Pro	gress:
Enable real-time ISP	to allow background pro	ogramming (for MAX II and	d MAX V devices)		
🔊 🔊 Start	File	Device	Checksum	Usercode	Progran Configu
Stop	led1.sof	EP2C5Q208	0006D730	FFFFFFF	
Auto Detect					
X Delete					
Add File					
	4				۱.
Save Hie					-
Add Device		<u></u>			
	TDI				
Down					-

Select a programming hardware setup applies only t	settings re setup to use when prog o the current programmer	ramming devices window.	. This programming
Currently selected hardware:	USB-Blaster [USB-0] No Hardware		•
Available hardware items	USB-Blaster [USB-0]		
Hardware	Server	Port	Add Hardware
			Remove Hardware

Click Close button. Back to programmer window, notice the selection of each red box in the picture below:

Programmer -	F:/wx2c8/01_led1/l	ed1 - led1 - [led1	cdf]*					×
<u>File E</u> dit <u>V</u> iew P <u>r</u>	ocessing <u>T</u> ools <u>W</u> indo	w Help 🛡						
Hardware Setup	USB laster [USB-0] P to allow background prog	M ramming (for MAX II and	ode: JTAG MAX V devices)	[Pegress:			
Start	5 File	Device	Checksum	Usercode	Program/ Verify Configure	Blank- Check	Examine	Se
Stop	ed1.sof	EP2C8Q208	000BEE9A	FFFFFFF				I
Auto Detect								
Add File	3							
Change File	•		Ш					•
Save File								-
Add Device								
🕐 Up								≡
Down								
	EP2C8C	208						
	↓ TDO							-

(1) Hardware setup, it has been set up in the previous step

(2) Select JTAG mode, and connect usb blaster cable to the JTAG port of the FPGA board .

(3) ADD File, select the .sof file.

(4) Program configure mark $\sqrt{}$.

(5) Click START.

After clicking the button start, the configuration LED of FPGA board will flash, and then the program started to run, eight LED lights lit at the same time.

3 Download via AS interface and configure EPCS chip

Through the AS interface to download the program code, the program is not lost after power down.

🔖 Programmer -	F:/wx2c8/01_led1/l	ed1 - led1 - [led1	.cdf]*					ا مہار ہے۔	x
Eile Edit View Pr	oc <mark>es</mark> ing <u>T</u> ools <u>W</u> indo	w Help 🛡			2				
Hardware Setup	. USB-Blaster [USB-0]	(1	ode: Active Seria	Programming	Progress				
Enable real-time ISF	o to allow background prog	ramming (for MAX II and	MAX V devices)						
Start	5 File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Se
Stop	led1.pof	EPCS16	1ED85815	00000000					
Auto Detect				4	-				
X Delete									
Add File	3								
									-
Change File	4		III						•
Save File									-
Add Device									
🜓 Up		RA							=
- Down	ASDI +								
	EPCS	16							
									*
									1.1

- (1) Hardware setup, select USB blaster.
- (2) Select AS mode, and connect usb blaster cable to the AS port of the FPGA board.
- (3) ADD File, select the .pof file.
- (4) Program configure mark $\sqrt{}$.
- (5) Click START.

Note: After downloading program via AS port, you need to turn off the power of the FPGA board, unplug the USB blaster from the AS port, and then re-power the FPGA board, run the program.